Docket No.: A8319.0004/P004
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Hiroshi Kageyama et al

Application No.: 09/938,614 Group Art Unit: 2673

Filed: August 27, 2001 Examiner: L. Shapiro

For: DRIVE CIRCUIT AND IMAGE DISPLAY APPARATUS

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REQUEST FOR RECONSIDERATION

Dear Sir:

In response to the Office action dated September 12, 2003 (paper no. 6), please consider the following remarks and arguments.

Claims 1-52 are pending in the present application. All pending claims stand rejected. Reconsideration and withdrawal of the pending rejections, in light of the following remarks and arguments, is respectfully solicited.

An interview was conducted at the Patent and Trademark Office on January 8, 2004. The interview was conducted between the Examiner and Primary Examiner in the instant case and Applicant's representative. During the interview, the pending rejections of the independent claims under 37 C.F.R. § 1.112 and § 1.103 (a) were considered in light of United States patent number 5,952,948 to Proebsting and United States patent number 6,335,721 to Jeong. A copy of the corresponding Interview Summary, prepared by the Examiner, is attached hereto.

Claims 1-52 stand rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement. Applicant respectfully traverses the rejection.

With respect to independent claims 1, 3, 9 and 11, the Office Action suggests that the limitation "a resistance within said sampling circuit" is unsupported by the specification. However, the specification states in the paragraph found on page 29 between lines 17 and 21 "[t]he resistance values R1, R2, and R3 of the thin-film transistors 26 and 27 and the resistance values Rsw of the conducting thin-film transistors 29 are inserted between the voltage dividing points and reference voltages," (emphasis added). Figure 2 shows transistors 29 within sampling circuit 23. Page 21, line 7. Accordingly, the subject claim limitation is fully supported by the specification.

With respect to independent claims 2, 4, 10 and 12, the limitation of "sampling switching elements divide any reference voltages as they are being output," is also fully supported by the specification. With reference to Fig. 2, applicant notes that, in one embodiment, the sampling switching elements (e.g., S1) are applied in pairs with the

signal line (e.g., SL1) electrically coupled between a first and a second of the sampling switching elements. The "sampling switching elements divide any reference voltages as they are being output."

Claims 1-20, 25-44 and 49-52 stand rejected under 35 U.S.C. § 103 (a) as being unpatentable over Proebsting in view of Jeong and in further view of United States patent number 5,608,421 to Okada. As demonstrated below, however, the proposed combination of Proebsting, Jeong and Okada does not anticipate claim 1 or render it obvious.

The present invention discloses a drive circuit comprising a plurality of DA converters and a plurality of sampling circuits. The sampling circuit selects one or two output voltages from the plurality of DA converters to output to one signal line. If two output voltages are selected, an intermediate voltage is made from the two output voltages.

In Fig. 2, a plurality of DA converters corresponds to the reference numbers 21 and 22 and a sampling circuit corresponds to the reference number 23. For example, in the case of outputting an intermediate voltage taken from a reference voltage V0 and a reference voltage V1 to a signal line SL1,

TFT (in a DA converter 21) between a node V0 and a node T1,

TFT (in a sampling circuit 23) between a node T1 and node SL1,

TFT (in a sampling circuit 23) between a node SL1 and a node T2 and

TFT (in a DA converter 22) between a node T2 and a node V1

are turned on, whereby a divisional voltage is outputted by use of on-resistance of each TFT.

FIG. 4 shows an equivalent circuit in which a voltage VSL occurs on signal lines SL1-SL4 in Fig. 2. In the case of IN=1 to 3, an intermediate voltage by a voltage division occurs. Each resistance value R1-R3 of a TFT in the DAC is connected to each resistance value RSW in series to divide the reference voltages Vn and Vn+1 (for example, V0 and V1) whereby an intermediate voltage occurs.

Therefore, in Fig. 2, a divisional voltage on the signal line occurs by the use of serial resistances comprising resistance values R1-R3 of TFTs in a DA converter and resistance values RSW of TFTs constituting a sampling circuit. Proebsting discloses a DA converter made to divide by the use of a resistance in a switch. However, Proebsting does not comprise a sampling circuit nor a means for dividing by the use of a resistance of a TFT in a sampling circuit.

Jeong discloses that, as shown in Fig. 2, an Output Buffer Circuit is connected to two DA converters and two Sample & Hold circuits. However, the Output Buffer Circuit outputs alternatively from either of two Sample & Hold circuits, to switch a voltage polarity applied to a Liquid Crystal. That is, the invention disclosed by Jeong cannot divide a voltage by use of a sampling circuit.

Okada discloses, as shown in Fig. 1, two DA converters DA1 and DA2, and a plurality of Signal voltage hold circuits M01-M04. However, a DA converter which is connected to one signal voltage hold circuit is either DA1 or DA2. That is, Okada does not disclose that each voltage of two DA converters is being divided. Further, Fig. 16 shows a circuit but the circuit shown in Fig. 1 does not have a component for dividing a voltage because only one reference voltage is shown.

A drive circuit assumed from the above three cited references would comprise two DACs made to divide by use of switch resistances, a plurality of Sample & Hold circuits or a signal voltage hold circuit, and a drive circuit having an output buffer circuit which selects alternative output voltages. This arrangement does not teach or suggest the present invention in which a voltage is divided by use of resistance of TFTs in a sampling circuit.

Put another way, claim 1 includes a unique combination of elements that is patentably distinguishable over the prior art including the limitations of "a sampling circuit which connects said first output terminal to a plurality of signal lines one by one in response to a signal line selection signal... wherein... [a] reference voltage selected... [is] output to said signal lines via the resistor inserted into any one of said circuits and a resistance within said sampling circuit." Proebsting relates to a digital to analog converter that "uses a dedicated resistive divider chain that is selectively switched between adjacent pairs of coarse analog reference signals to generate finer analog reference signals."

The Proebsting reference does not teach or suggest a sampling circuit, and the Office Action asserts that the Jeong reference provides this element. Specifically, the Office Action relies on elements 30, 64 and 56 in figures 2 and 3 of Jeong and notes that Fig. 3 shows a circuit of the output buffer 64. The output buffer 64, however, has only a single output. Accordingly, it does not teach or suggest "a sampling circuit which connects said first output terminal to a plurality of signal lines... and connects said second output terminal to said plurality of signal lines."

The proposed combination of Proebsting and Jeong also does not teach or suggest a "reference voltage... output to said signal lines via the resistor inserted into any of said circuits and a resistance within said sampling circuit." The Office Action

attempts to overcome this further deficiency by combining Proebsting and Jeong with Okada.

As noted above, Jeong does not teach or suggest a sampling circuit, as claimed. Therefore there is no basis on which to suggest that the resistance of Okada could be combined therein. Moreover, the combination including Okada does not teach or suggest a resistance within a sampling circuit wherein the sampling circuit "connects said first output terminal to a plurality of signal lines... and connects said second output terminal to said plurality of signal lines." As shown in Fig. 4, the output terminals of Okada are connected to different pluralities of signal lines.

Accordingly, the references, whether taken alone or in combination, do not teach or suggest all of the limitations of claim 1. Therefore the proposed combination of Proebsting, Jeong and Okada does not anticipate claim 1 or render it obvious, and the rejection of claim 1 under 35 U.S.C. § 103 should be withdrawn.

Even if, *arguendo*, Proebsting, Jeong and Okada together contained every element of claim 1, there is no proper basis for making the proposed combination. In order to combine references, there must be a teaching or suggestion in the prior art to support the proposed combination.

The Office Action posits that the combination of Proebsting and Jeong is suggested by the statement in Proebsting that there is "a need for an LCD column driver circuit that consumes less power and area." However, there is nothing in the prior art that would lead one from this assertion to a combination of the Proebsting and Jeong references.

The Jeong reference relates to "a liquid crystal display (LCD) source driver with increased current driving capacity for driving the LCD and converting digital

video signals into positive and negative analog video signals for an inversion method." Column 1, lines 9-13. Jeong also discusses reduction in "flicker." Column 1, lines 49-51.

Jeong does not teach or suggest "an LCD column driver circuit that consumes less power and area." Accordingly, the mere assertion in Proebsting that such an LCD column driver is desirable would not lead one of skill in the art to combine Proebsting with Jeong. Therefore, the Office Action's conclusions of obviousness appear to be based upon impermissible hindsight by using the claims of the present invention as a road map to improperly modify the cited references.

With respect to claim 2, the proposed combination of Proebsting, Jeong and Okada does not teach or suggest "a sampling circuit which has a first group of sampling switching elements inserted between said first output terminal and a plurality of signal lines and a second group of sampling switching elements inserted between said second output terminal and said plurality of signal lines." Nor does the combination teach "conducting switching elements... wherein said sampling switching elements divide any reference voltages as they are being output," since the switching elements of Okada are not connected in pairs. Therefore, the rejection of claim 2 withdrawn.

With respect to claim 3, the combined references do not teach or suggest "a sampling circuit which connects said first output terminal to a plurality of signal lines... and connects said second output terminal to said plurality of signal lines." With respect to claim 4, the combined references do not teach or suggest "a sampling circuit which has a first group of sampling switching elements inserted between said first output terminal and a plurality of signal lines and a second group of sampling signal elements inserted between said second output terminal and said plurality of signal lines." Accordingly, the rejections of claims 3 and 4 should also be withdrawn.

The rejections of claims 9-12 under 35 U.S.C. § 103 (a) over Proebsting in view of Jeong and Okada should be withdrawn for at least reasons similar to those presented above in relation to the rejections of claims 1-4.

Claims 5-8, 13-20, 25-44 and 49-52 each respectively depend, directly or indirectly, from claims 1-4 and 9-12 and incorporate the respective limitations thereof. Accordingly, the rejections of claims 5-8, 13-20, 25-44 and 49-52 under 35 U.S.C. § 103 (a) over Proebsting in view of Jeong and Okada should be withdrawn for at least the reasons given above in relation to claims 1-4 and 9-12.

Claims 21-24 and 45-48 stand rejected under 35 U.S.C. § 103 (a) as being unpatentable over Proebsting in view of Jeong and Okada and in further view of United States patent number 6,411,273 to Nakamura (Nakamura). The Office Action acknowledges that Proebsting, Jeong and Okada do not teach or suggest the limitation of using thin film transistors as claimed, and Nakamura is proposed to be added to the combination to overcome this further deficiency. However, claims 21-24 and 45-48 depend respectively from independent claims 1-4 and 9-12.

Therefore, as discussed above in relation to claims 1-4 and 9-12 additional limitations of the subject claims are absent from the prior art. Inasmuch as Nakamura does not teach or suggest these additional limitations, the proposed combination of Proebsting, Jeong, Okada and Nakamura does not anticipate claims 21-24 and 45-48. Therefore the rejections of these claims should also be withdrawn.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue.

Dated: 12 JAN 2004

Respectfully submitted,

By _____

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